REGNAME.IAA(03-Jul-90) Latest regname for Hi-Res chips

&=Register used by DMA channel only.
%=Register used by DMA channel usually, processors sometimes.
+=Address register pair.Low word uses DB1-DB15,High word DB0-DB4.
~=Address not writable by the Coprocessor unless COPCON bit 1 is set true.
h=new for HiRes chip set
p=new for IAA chip set
A=Agnus chip, D=Denise chip, P=Paula chip
W=Write, R=Read,
ER=Early read. This is a DMA data transfer to RAM, from either the Disk
or from the Blitter . Ram timing requires data to be on the bus
earlier than microprocessor read cycles. These transfers are therefore
initiated by Agnus timing, rather than a read address on the
register address bus (RGA).
S=Strobe (write address with no register bits)
PTL,PTH=20 bit Pointer that addresses DMA data. Must be reloaded by a processor
before use (Vertical blank for Bit Plane and Sprite pointers, and
prior to starting the Blitter for Blitter pointers).(old chips- 18 bits)
LCL,LCH=20 bit Location (starting address) of DMA data. Used to automaticall
restart pointers, such as the Coprocessor program counter (during
vertical blank), and the Audio sample counter (whenever the audio
length count is finished) (Old chips- 18 bits)
MOD=15 bit Modulo. A number that is automatically added to the memory address
at the end of each line to generate the address for the beginning of
the next line. This allows the Blitter (or the Display Window) to
operate on (or display) a window of data that is smaller than the
actual picture in memory. (memory map) Uses 15 bits, plus sign extend.

NAME		ADD	R/W	CHIP		FUNCTION
BLTDDAT	&	~000	ER	A		Blitter dest. early read (dummy address)
DMACONR		~002	R	A	P	DMA control (and blitter status) read
VPOSR		~004	R	A		Read Vert most sig. bits (and frame flop)
VHPOSR		~006	R	A		Read Vert and horiz Position of beam
DSKDATR	&	~008	ER		P	Disk data early read (dummy address)
JOY0DAT		~00A	R	D		Joystick-mouse 0 data (vert,horiz)
JOY1DAT		~00C	R	D		Joystick-mouse 1 data (vert,horiz)
CLXDAT		~00E	R	D		Collision data reg.(Read and clear)
ADKCONR		~010	R		P	Audio, disk control register read
POT0DAT		~012	R		P	Pot counter pair 0 data (vert,horiz)
POT1DAT		~014	R		P	Pot counter pair 1 data (vert,horiz)
POTINP		~016	R		P	Pot pin data read
SERDATR		~018	R		P	Serial Port Data and Status read
DSKBYTR		~01A	R		P	Disk Data byte and status read
INTENAR		~01C	R		P	Interrupt Enable bits Read
INTREQR		~01E	R		P	Interrupt Request bits read
DSKPTH	+	~020	W	A		Disk pointer (High 5 bits)
DSKPTL	+	~022	W	A		Disk pointer (Low 15 bits)
DSKLEN		~024	W		P	Disk length
DSKDAT	&	~026	W		P	Disk DMA Data write
REFPTR	&	~028	W	A		Refresh pointer
VPOSW		~02A	W	A		Write Vert most sig. bits (and frame flop)
VHPOSW		~02C	W	A		Write Vert and horiz Position of beam
COPCON		~02E	W	A		Coprocessor control register (CDANG)
SERDAT		~030	W		P	Serial Port Data and stop bits write
SERPER		~032	W		P	Serial Port Period and control
POTGO		~034	W		P	Pot count start,pot pin drive enable and data
JOYTEST		~036	W	D		Write to all 4 Joystick-mouse counters at once.
STREQU	&	~038	S	D		Strobe for horiz sync with VB and EQU
STRVBL	&	~03A	S	D		Strobe for horiz sync with VB (Vert. Blank)

STRHOR	&	~03C	S		D	P	Strobe for horiz sync
STRLONG	&	~03E	S		D		Strobe for identification of long horz. line.
BLTCON0		~040	W	A			Blitter control register 0
BLTCON1		~042	W	A			Blitter control register 1
BLTAFWM		~044	W	A			Blitter first word mask for source A
BLTALWM		~046	W	A			Blitter last word mask for source A
BLTCPTH	+	~048	W	A			Blitter Pointer to source C (High 5 bits)
BLTCPTL	+	~04A	W	A			Blitter Pointer to source C (Low 15 bits)
BLTBPTH	+	~04C	W	A			Blitter pointer to source B (High 5 bits)
BLTBPTL	+	~04E	W	A			Blitter pointer to source B (Low 15 bits)
BLTAPTH	+	~050	W	A			Blitter Pointer to source A (High 5 bits)
BLTAPTL	+	~052	W	A			Blitter Pointer to source A (Low 15 bits)
BLTDPTH	+	~054	W	A			Blitter Pointer to destn. D (High 5 bits)
BLTDPTL	+	~056	W	A			Blitter Pointer to destn. D (Low 15 bits)
BLTSIZE		~058	W	A			Blitter start and size (window width, height)
BLTCON0L	h	~05A	W	A			Blitter control 0 lower 8 bits(minterms)
BLTSIZV	h	~05C	W	A			Blitter V size (for 15 bit vert size)
BLTSIZH	h	~05E	W	A			Blitter H size & start (for 11 bit H size)
BLTCMOD		~060	W	A			Blitter Modulo for source C
BLTBMOD		~062	W	A			Blitter Modulo for source B
BLTAMOD		~064	W	A			Blitter Modulo for source A
BLTDMOD		~066	W	A			Blitter Modulo for destn. D
		~068					
		~06A					
		~06C					
		~06E					
BLTCDAT	&	~070	W	A			Blitter source C data reg
BLTBDAT	&	~072	W	A			Blitter source B data reg
BLTADAT	&	~074	W	A			Blitter source A data reg
FMODE	p	~076	W	AD			Fetch MODE register
SPRHDAT	&h	078	W	A			ext logic UHRES sprite pointer & data identifier
(BPLHDAT)		~07A					
DENISEID	h	~07C	R		D		Chip Revision level for Denise (video out chip)
DSKSYNC		~07E	W			P	Disk sync pattern register for disk read.
COP1LCH	+	080	W	A			Coprocessor first location reg (High 5 bits)
COP1LCL	+	082	W	A			Coprocessor first location reg. (Low 15 bits)
COP2LCH	+	084	W	A			Coprocessor second location reg. (High 5 bits)
COP2LCL	+	086	W	A			Coprocessor second location reg(Low 15 bits)
COPJMP1		088	S	A			Coprocessor restart at first location
COPJMP2		08A	S	A			Coprocessor restart at second location
COPINS		08C	W	A			Coprocessor inst. fetch identify
DIWSTRT		08E	W	A	D		Display Window Start (upper left vert-hor pos)
DIWSTOP		090	W	A	D		Display Window Stop (lower right vert-hor pos)
DDFSTRT		092	W	A			Display bit plane data fetch start(hor pos)
DDFSTOP		094	W	A			Display bit plane data fetch stop(hor pos)
DMACON		096	W	A		P	DMA control write(clear or set)
CLXCON		098	W		D		Collision control
INTENA		09A	W			P	Interrupt Enable bits (clear or set bits)
INTREQ		09C	W			P	Interrupt Request bits (clear or set bits)
ADKCON		09E	W			P	Audio, Disk, UART, Control
AUD0LCH	+	0A0	W	A			Audio channel 0 location (High 5 bits)
AUD0LCL	+	0A2	W	A			Audio channel 0 location (Low 15 bits)
AUD0LEN		0A4	W			P	Audio Channel 0 length
AUD0PER		0A6	W			P	Audio channel 0 Period
AUD0VOL		0A8	W			P	Audio Channel 0 Volume
AUD0DAT	&	0AA	W			P	Audio channel 0 Data
		0AC					
		0AE					
AUD1LCH	+	0B0	W	A			Audio channel 1 location (High 5 bits)
AUD1LCL	+	0B2	W	A			Audio channel 1 location (Low 15 bits)
AUD1LEN		0B4	W			P	Audio Channel 1 length

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AUD1PER      0B6  W       P   Audio channel 1 Period
AUD1VOL      0B8  W       P   Audio Channel 1 Volume
AUD1DAT   &  0BA  W       P   Audio channel 1 Data
             0BC
             0BE
AUD2LCH   +  0C0  W   A       Audio channel 2 location (High 5 bits)
AUD2LCL   +  0C2  W   A       Audio channel 2 location (Low 15 bits)
AUD2LEN      0C4  W       P   Audio Channel 2 length
AUD2PER      0C6  W       P   Audio channel 2 Period
AUD2VOL      0C8  W       P   Audio Channel 2 Volume
AUD2DAT   &  0CA  W       P   Audio channel 2 Data
             0CC
             0CE
AUD3LCH   +  0D0  W   A       Audio channel 3 location (High 5 bits)
AUD3LCL   +  0D2  W   A       Audio channel 3 location (Low 15 bits)
AUD3LEN      0D4  W       P   Audio Channel 3 length
AUD3PER      0D6  W       P   Audio channel 3 Period
AUD3VOL      0D8  W       P   Audio Channel 3 Volume
AUD3DAT   &  0DA  W       P   Audio channel 3 Data
             0DC
             0DE
BPL1PTH   +  0E0  W   A       Bit plane 1 pointer (High 5 bits)
BPL1PTL   +  0E2  W   A       Bit plane 1 pointer (Low 15 bits)
BPL2PTH   +  0E4  W   A       Bit plane 2 pointer (High 5 bits)
BPL2PTL   +  0E6  W   A       Bit plane 2 pointer (Low 15 bits)
BPL3PTH   +  0E8  W   A       Bit plane 3 pointer (High 5 bits)
BPL3PTL   +  0EA  W   A       Bit plane 3 pointer (Low 15 bits)
BPL4PTH   +  0EC  W   A       Bit plane 4 pointer (High 5 bits)
BPL4PTL   +  0EE  W   A       Bit plane 4 pointer (Low 15 bits)
BPL5PTH   +  0F0  W   A       Bit plane 5 pointer (High 5 bits)
BPL5PTL   +  0F2  W   A       Bit plane 5 pointer (Low 15 bits)
BPL6PTH   +  0F4  W   A       Bit plane 6 pointer (High 5 bits)
BPL6PTL   +  0F6  W   A       Bit plane 6 pointer (Low 15 bits)
BPL7PTH      0F8
BPL7PTL      0FA
BPL8PTH      0FC
BPL8PTL      0FE
BPLCON0      100  W   A D     Bit plane control register(misc control bits)
BPLCON1      102  W     D     Bit plane control reg (scroll value PF1, PF2)
BPLCON2      104  W     D     Bit plane control reg (priority control)
BPLCON3      106  W     D     Bit plane control reg (enhanced features)
BPL1MOD      108  W   A       Bit plane modulo (odd planes)
BPL2MOD      10A  W   A       Bit Plane modulo (even planes)
BPLCON4   p  10C  W     D     Bit plane control reg (bitplane and sprite masks)
CLXCON2   p  10E  W     D     Extended collision control register
BPL1DAT   &  110  W     D     Bit plane 1 data (Parallel to serial convert)
BPL2DAT   &  112  W     D     Bit plane 2 data (Parallel to serial convert)
BPL3DAT   &  114  W     D     Bit plane 3 data (Parallel to serial convert)
BPL4DAT   &  116  W     D     Bit plane 4 data (Parallel to serial convert)
BPL5DAT   &  118  W     D     Bit plane 5 data (Parallel to serial convert)
BPL6DAT   &  11A  W     D     Bit plane 6 data (Parallel to serial convert)
BPL7DAT   &p 11C  W     D     Bit plane 7 data (Parallel to serial convert)
BPL8DAT   &p 11E  W     D     Bit plane 8 data (Parallel to serial convert)
SPR0PTH   +  120  W   A       Sprite 0 pointer (High 5 bits)
SPR0PTL   +  122  W   A       Sprite 0 pointer (Low 15 bits)
SPR1PTH   +  124  W   A       Sprite 1 pointer (High 5 bits)
SPR1PTL   +  126  W   A       Sprite 1 pointer (Low 15 bits)
SPR2PTH   +  128  W   A       Sprite 2 pointer (High 5 bits)
SPR2PTL   +  12A  W   A       Sprite 2 pointer (Low 15 bits)
SPR3PTH   +  12C  W   A       Sprite 3 pointer (High 5 bits)
SPR3PTL   +  12E  W   A       Sprite 3 pointer (Low 15 bits)
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SPR4PTH	+	130	W	A		Sprite 4 pointer (High 5 bits)
SPR4PTL	+	132	W	A		Sprite 4 pointer (Low 15 bits)
SPR5PTH	+	134	W	A		Sprite 5 pointer (High 5 bits)
SPR5PTL	+	136	W	A		Sprite 5 pointer (Low 15 bits)
SPR6PTH	+	138	W	A		Sprite 6 pointer (High 5 bits)
SPR6PTL	+	13A	W	A		Sprite 6 pointer (Low 15 bits)
SPR7PTH	+	13C	W	A		Sprite 7 pointer (High 5 bits)
SPR7PTL	+	13E	W	A		Sprite 7 pointer (Low 15 bits)
SPR0POS	%	140	W	A	D	Sprite 0 Vert-Horiz start position data
SPR0CTL	%	142	W	A	D	Sprite 0 position and control data
SPR0DATA	%	144	W		D	Sprite 0 image data register A
SPR0DATB	%	146	W		D	Sprite 0 image data register B
SPR1POS	%	148	W	A	D	Sprite 1 Vert-Horiz start position data
SPR1CTL	%	14A	W	A	D	Sprite 1 position and control data
SPR1DATA	%	14C	W		D	Sprite 1 image data register A
SPR1DATB	%	14E	W		D	Sprite 1 image data register B
SPR2POS	%	150	W	A	D	Sprite 2 Vert-Horiz start position data
SPR2CTL	%	152	W	A	D	Sprite 2 position and control data
SPR2DATA	%	154	W		D	Sprite 2 image data register A
SPR2DATB	%	156	W		D	Sprite 2 image data register B
SPR3POS	%	158	W	A	D	Sprite 3 Vert-Horiz start position data
SPR3CTL	%	15A	W	A	D	Sprite 3 position and control data
SPR3DATA	%	15C	W		D	Sprite 3 image data register A
SPR3DATB	%	15E	W		D	Sprite 3 image data register B
SPR4POS	%	160	W	A	D	Sprite 4 Vert-Horiz start position data
SPR4CTL	%	162	W	A	D	Sprite 4 position and control data
SPR4DATA	%	164	W		D	Sprite 4 image data register A
SPR4DATB	%	166	W		D	Sprite 4 image data register B
SPR5POS	%	168	W	A	D	Sprite 5 Vert-Horiz start position data
SPR5CTL	%	16A	W	A	D	Sprite 5 position and control data
SPR5DATA	%	16C	W		D	Sprite 5 image data register A
SPR5DATB	%	16E	W		D	Sprite 5 image data register B
SPR6POS	%	170	W	A	D	Sprite 6 Vert-Horiz start position data
SPR6CTL	%	172	W	A	D	Sprite 6 position and control data
SPR6DATA	%	174	W		D	Sprite 6 image data register A
SPR6DATB	%	176	W		D	Sprite 6 image data register B
SPR7POS	%	178	W	A	D	Sprite 7 Vert-Horiz start position data
SPR7CTL	%	17A	W	A	D	Sprite 7 position and control data
SPR7DATA	%	17C	W		D	Sprite 7 image data register A
SPR7DATB	%	17E	W		D	Sprite 7 image data register B
COLOR00		180	W		D	Color table 00
COLOR01		182	W		D	Color table 01
COLOR02		184	W		D	Color table 02
COLOR03		186	W		D	Color table 03
COLOR04		188	W		D	Color table 04
COLOR05		18A	W		D	Color table 05
COLOR06		18C	W		D	Color table 06
COLOR07		18E	W		D	Color table 07
COLOR08		190	W		D	Color table 08
COLOR09		192	W		D	Color table 09
COLOR10		194	W		D	Color table 10
COLOR11		196	W		D	Color table 11
COLOR12		198	W		D	Color table 12
COLOR13		19A	W		D	Color table 13
COLOR14		19C	W		D	Color table 14
COLOR15		19E	W		D	Color table 15
COLOR16		1A0	W		D	Color table 16
COLOR17		1A2	W		D	Color table 17
COLOR18		1A4	W		D	Color table 18
COLOR19		1A6	W		D	Color table 19
COLOR20		1A8	W		D	Color table 20

COLOR21		1AA	W		D	Color table 21
COLOR22		1AC	W		D	Color table 22
COLOR23		1AE	W		D	Color table 23
COLOR24		1B0	W		D	Color table 24
COLOR25		1B2	W		D	Color table 25
COLOR26		1B4	W		D	Color table 26
COLOR27		1B6	W		D	Color table 27
COLOR28		1B8	W		D	Color table 28
COLOR29		1BA	W		D	Color table 29
COLOR30		1BC	W		D	Color table 30
COLOR31		1BE	W		D	Color table 31
HTOTAL	h	1C0	W	A		Highest number count in horiz line (VARBEAMEN=1)
HSSTOP	h	1C2	W	A		Horiz line pos for HSYNC stop
HBSTRT	h	1C4	W	A		Horiz line pos for HBLANK start
HBSTOP	h	1C6	W	A		Horiz line pos for HBLANK stop
VTOTAL	h	1C8	W	A		Highest numbered Vertical line (VARBEAMEN=1)
VSSTOP	h	1CA	W	A		Vert. line pos for VSYNC stop
VBSTRT	h	1CC	W	A		Vert line for VBLANK start
VBSTOP	h	1CE	W	A		Vert line for VBLANK stop
SPRHSTRT	h	1D0	W	A		UHRES sprite vertical start
SPRHSTOP	h	1D2	W	A		UHRES sprite vertical stop
BPLHSTRT	h	1D4	W	A		UHRES bit plane vertical start
BPLHSTOP	h	1D6	W	A		UHRES bit plane vertical stop
HHPOSW	h	1D8	W	A		DUAL mode hires H beam counter write
HHPOSR	h	1DA	R	A		DUAL mode hires H beam counter read
BEAMCON0	h	1DC	W	A		Beam counter control register(SHRES,UHRES,PAL)
HSSTRT	h	1DE	W	A		Horizontal Sync start (VARHSY)
VSSTRT	h	1E0	W	A		Vertical Sync start (VARVSY)
HCENTER	h	1E2	W	A		Horizontal position for Vsync on interlace
DIWHIGH	h	~1E4	W	A	D	Display window- upper bits for start,stop
BPLHMOD	h	1E6	W	A		UHRES bit plane modulo
SPRHPTH	+h	1E8	W	A		UHRES sprite pointer (High 5 bits)
SPRHPTL	+h	1EA	W	A		UHRES sprite pointer (Low 15 bits)
BPLHPTH	+h	1EC	W	A		VRam (UHRES) bit plane pointer (High 5 bits)
BPLHPTL	+h	1EE	W	A		VRam (UHRES) bit plane pointer (Low 15 bits)
RESERVED		1F0-1FC				
NO-OP(NULL)		1FE				Can also indicate last 2 or 3 refresh cycles or the restart of the COPPER after lockup.