# The A3000 Local Bus Expansion Slot Specification

A High Performance Expansion Slot specific
to Amiga 3000 family computers

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# CHAPTER 1

## INTRODUCTION

*"What works for me might work for you"*
*-Jimmy Buffett*

This document describes the Amiga 3000 Local Bus Expansion Slot, also known as the Amiga 3000 Coprocessor Slot. This expansion slot is designed to provide high speed access to the Amiga 3000's local, or 68030, bus. This slot is intended for high speed expansion devices that are generally very specific to the 68030 bus or need direct access to the local bus for other reasons. Such devices include alternate 680x0 family processors, cache memory boards, high speed bursting ram expansion, and similar things.

### 1.1 Intended Audience

This document is written for hardware engineers interested in designing cards for the Amiga 3000's Local Bus Slot. A good level of microcomputer systems design knowledge is necessary to get much meaning out of these pages. Especially important is familiarity with the 68030 processor hardware conventions, as most of the Local Bus Slot is based directly on the 68030 processor bus.

### 1.2 Why a Local Bus Slot?

The local bus slot was originally introduced on the Amiga 2000, and has served its intended purpose quite well on that system. We expect the A3000's Local Bus Slot to provide similar functionality on the A3000.

The main use for the Local Bus Slot is the addition of a single, very tightly coupled expansion device, which is typically a high speed CPU, cache, or memory board. An alternate 680x0 family device, such as a 68040 processor, needs access to every 68030 signal in order to properly replace the 68030 processor as a host for AmigaOS or UNIX. Cache memories or extremely fast "Fast" memory needs direct access to the 68030 bus to run as tighly coupled as possible to the 68030 processor on the A3000's motherboard. Most other devices expansion devices are expected to be designed as Zorro II or Zorro III expansion cards.

In any system design, you can make good arguments for a general purpose expansion bus, and good arguments for an extendable local bus. The Amiga philosophy is that both of these approaches are correct, and seve complementary needs. Any of the stated candidates for the Local Bus Slot are by their very nature tightly coupled to the A3000's system bus, which is of course based on the 68030 bus. They are not expected to work in future Amiga systems, which could easily have completely different local buses, and therefore, different local bus slots. Also, it's impractical to provide a large number of such slots, since the local bus itself has tight electrical limits on expandability, yet any buffers imposed between the local bus and Local Bus Slot devices can reduce the high performance we're striving for. So a single local bus slot is provided.

### 1.3 Why an Expansion Bus Slot?

Most Amiga 3000 add-on cards belong in an Expansion Bus Slot. First of all, since there is only one Local Bus Slot, it stands to reason that only one such device can be added to any system, while at least four Expansion Bus (Zorro III) slots are available on any A3000 family computer, and can be expected on any more advanced architure Amiga in the future. The Zorro III bus doesn't permit the same degree of tight coupling that the Local Bus Slot does, so its not capable of supporting cache or other zero wait-state memory, and it can't support a direct-replacement 68040. It does permit reasonable speeds, interrupts, bus locking, etc. so it is the place for high performance I/O devices, moderate speed add-on memory boards, processor devices such as DSP, Video, or RISC devices that coexist with the main processor, etc. And of course, devices that are happy as slower 16 bit peripherals can be implemented as Zorro II cards and have the advantage of working in all Amiga computers (including the A500 and A1000 with the proper 3rd party bus adaptor or backplane). Details on the Zorro III bus are available in *The Zorro III Expansion Bus Specification*, while the Zorro II bus is described in *The A500/A2000 Technical Reference Manual*.

### 1.4 The Amiga 3000 Family

There are three basic Amiga 3000 class machines: the original Amiga 3000, the Amiga 3000T, and the Amiga 3000+. Some enhancements to the original A3000 Local Bus Slot were added to the A3000T, mainly signals associated with the jumper-less clock takeover mechanism. These are described in section 3.7. Additional enhancements were added for the A3000+; these are described in section 3.8.

# CHAPTER 2

## FUNCTIONALITY AND DESIGN GUIDELINES

*"Time and distance are out of place here"*

*-REM*

The Amiga 3000 Local Bus Expansion Slot provides signals to implement both slave and master devices. Memory devices, including cache, are bus slaves, while CPU devices such are 680x0 accelerator boards are bus masters. Any card may, at times, be either slave or master, and in a few cases, both at once.

### 2.1 Slave Devices

A slave device is a device that responds to the current local bus master. The local connector provides direct access to all local bus signals, which include all 68030 signals, plus a few additional Amiga 3000 specific lines to allow a Local Bus Slot device to control the A3000's Local Bus. Local Bus Slot slaves are not autoconfigured as are Zorro III bus devices, but instead are fixed in the address range from $08000000 to $0fffffff. The A3000 local bus controller, the Fat Gary chip, provides a decode of this space on the signal /RAMSLOT which is valid at address time. This signal may be ignored and the address decoded by logic on the board if speed is an issue. Local slave devices should also support the signal /CIIN if they contain uncachable data. The Amiga OS expects anything mapped starting at $08000000 to be memory, and in fact, the fastest memory in the A3000 system. The OS will automatically size and link in any memory it finds here, and place it in the system as the highest priority memory available. To support control registers or other memory mapped resources on a Local Bus Card, locate them at least 512K above the $08000000 base, and the OS will ignore them.

A signal named /WAIT is provided for cache support. Asserting this signal will disable address decoding of onboard Fast RAM by the RAMSEY chip and Zorro II/III bus accesses by the BUSTER chip. Constraints imposed by the 68030 allow only 18ns to determine a cache hit. It is often more feasible to assert /STERM before knowing whether the cycle is a cache hit and rerunning the cycle via /HALT and /BERR if it is a miss. To achieve this functionality any decoding of the first cycle by RAMSEY or BUSTER must be disabled by asserting /WAIT less than 10ns after address valid. If the cycle is determined to miss a rerun is initiated and wait deasserted for the secondary cycle. Assertion of /WAIT will keep /STERM, /CBACK, etc. tristated by BUSTER or RAMSEY and may be controlled by the cache control logic.

## 2.2 Master Devices

A Master Device is, of course, a device which masters the local bus, replacing the functions of the 68030 during its period of mastership. Bus mastership may be accomplished two ways depending on the desired functionality. The first mode, called *primary mastership,* totally disables the motherboard 68030 and its arbitration logic, essentially replacing the 68030 with the local slot device. Such a device takes over full arbitration responsibility for the whole system, and must service all interrupts. The second mode, called *secondary mastership,* allows the on-board 68030 and the local bus accelerator board to share the bus, permitting multiprocessor capabilities or more traditional DMA from the local bus board. This protocol permits very fast switching between the local slot master and the motherboard 68030. In this mode, the 68030 is still responsible for bus arbitration.

### 2.2.1 Primary Bus Mastership

The primary bus mastership, or arbitration takeover mode, requires less logic to implement and may be preferred in most implementations. In the absence of multiprocessing software support, this is the mode of choice, and corresponds to the way in which most A2000 local slot cards worked.

The local bus card asserts /CBR at power on to the motherboard which in turn asserts /BR to the motherboard 68030. Upon receiving /BG30 from the motherboard the local card asserts /BOSS. Logic on the motherboard uses /BOSS to force /BGACK30 low to the 68030 only and not the shared local bus /BGACK. In addition the assertion of /BOSS tristates /BG on the motherboard and in turn the local card should untristate and source its /BG. The local card is now the default bus master and arbiter -- it must provide arbitration for the local bus, based on the 68030 bus arbitration rules. The onboard 68030 is bus arbitrated away and never regains the bus. Pal equations to implement this are given in *Figure 2-1,* all pal equations are active high and should be inverted in the output stage of the pal for active low assertion.

Actual timing for takeover mode is not given since all signals are inherently asychronous. The untristating of /BG should be later than the tristating of /BG on the motherboard to minimize contention on that signal.

```
/* Always assert Coprocessor Bus Request. */
CBR         =     'b'1;

/*  The Boss Signal. "poweron_reset" is a signal sourced by the local card and
   is asserted for a few hundred nanoseconds after poweron. This clears the
   feedback path on the pal and may be generated by an RC network which is
   slewrate cleaned by a schmitt trigger device. */
BOSS        =     BG30 # BOSS & !poweron_reset;

/*  The Grant Signal. "local_card_bg" is sourced by the local card in
   compliance to  the operation of arbitration defined in the 68030 users
   manual. */
BG          =     local_card_bg;

BG.oe       =     BOSS;
```

*Figure 2-1: Primary Mode Takeover PAL Equations*

### 2.2.2 Secondary Bus Mastership

The secondary bus acquisition mode uses the 68030 arbiter to provide cycle arbitration between the local slot card and the motherboard DMA. Since the 68030 provides only a single bus request input, a scheme referred to as fast arbitration is used between the local card and all other DMA sources, which are controlled via the BUSTER chip. Bus request is an open collector line which is time multiplexed between the local card and BUSTER. On a positive edge of CPUCLK, BUSTER will assert /BR if it requires the bus and /BR is not already asserted by the local bus card. On the negative transition of CPUCLK, the local bus card may assert /BR if it is not already asserted by BUSTER. This scheme allows both masters to share a single bus request and also requires only 20ns to resolve the master arbitration. This mode is very efficient but forces the local card to use high speed logic since the time between clock edges is so short. It is *strongly* suggested that the above logic be incorporated in a 7.5ns or faster registered PAL connected to a F38 open collector device. Clock skew between the clock to this pal and CPUCLK is critical and it is advised that the local card generate and source clocks to the motherboard, especially if CPUCLK is needed elsewhere on the card; load on CPUCLK at the Local Bus Slot must be kept to a minimum to avoid mucking with the local bus timing. Skew between CPUCLK and the clock driving this pal should be less than 2ns. The PAL equations for /BR are given in *Figure 2-2*.

After receiving /BG from the motherboard 68030 the local card drives /BGACK (open collector) and assumes mastership of the bus. It may keep the bus for multiple cycles but should not hog the bus for extended periods unless it relinquishes the bus when DMA request is asserted by BUSTER. Hogging the bus may cause adverse operation of the A3000. Be aware that the local bus signals must be tristated (/AS, /DSACK, Address, Data, etc.) prior to deasserting /BGACK. In addition the local card must not drive the bus or /BGACK until /AS, /DSACK, /BERR, /HALT, etc. have deasserted. In other words, standard 680x0 bus arbitration rules apply here. It is generally assumed that any secondary bus master mode Local Bus Slots device will be attempt to prevent undue bus hogging at the design level. This implies either a coprocessor device of

```
/*  This is the BR_LOCAL signal, which is an active output fed into a 74f38,
or other open collector equivalent buffer, to produce /BR.  /BR is the raw bus
   request from the local bus connector (keep this trace short on the local
   card).  WANTBUS is the request from the local card which deasserts after it
   sees BR_LOCAL asserted.  BGACK_LOCAL is /BGACK asserted by the local card.
   RESET is any reset signal used to prevent poweron latchup of BR_LOCAL. */

BR_LOCAL.d  =     !BR & !BR_LOCAL & WANTBUS
            #     BR_LOCAL & !BGACK_LOCAL & !RESET;
```

*Figure 2-2: Secondary Mode Takeover PAL Equations*

some kind that makes only periodic requests of the bus, or a CPU subsystem that contains its own local cache or memory. Any device that requires the mastering the local bus for very long periods of time should be a primary mode bus master.

It is extremely important that the bus master timing from the local card emulate operation of a 25MHZ or 16MHZ 68030 chip *exactly* as defined by the 68030 user manual. Future enhancements to the A3000 motherboard chips may incorporate rerun cycles and currently incorporate burst cycles and cache coherency signals (/CIIN). Signals received by the local card from the motherboard provide only the minimum setup and hold required by a 68030. Do not assume for example that data setup from the motherboard will not significantly change , ie. data setup from Fast RAM on subsequent cycles of a burst is much less than a typical non-burst cycle.

In addition to the 68030 specifications, the A3000 local bus adds one additional constraint. Slave devices should should hold data through the end of cycle, regardless of whether the cycle is terminated by /STERM or the /DSACK lines. In other words, only the current bus master really knows when a cycle has completed. Obviously, burst cycles are an exception to this; they follow the standard 68030 rules in dealing with data hold times.

### 2.3 Clock generation

The A3000 motherboard provides links to disable generation of CPUCLK and CLK90. This allows the local slot card to maintain better clock skew relationships between its own logic and that of the motherboard, and is especially important if the Local Bus card depends upon being synchronous to the A3000 motherboard clocks -- just as with the A2000 local bus slot, both synchronous and asynchronous designs are possible, but synchronous designs are much more timing critical than on the A2000.

If a local bus card drives the clock lines the appropriate jumpers must be moved on the motherboard. CLK90 must be a clock 90° out of phase from CPUCLK. It is typically generated from a 5 tap 25ns delay line where CLK90 is the 10ns tap when running the system at 25Mhz and CLK90 is the 15ns tap when at 16Mhz. Note that these clocks are fed through a 74f08 to provide clocking to the motherboard. If the skew generated by the f08 is unaccepable (as in fast arbitration) the socketed f08 may be removed and replaced by a header which shorts the

appropriate inputs to outputs, though it is the responsibility of the Local Bus card at that point to make sure acceptible versions of CPUCLK and CLK90 exist everywhere on the motherboard. Again careful layout of the clock circuitry is essential for reliable operation.

### 2.4 Local Bus Design Criteria

Any design which plugs into the local bus connector must comply to some basic design rules.

- Due to inductance in the 200pin connector to VCC and GND it is very imporant to provide ample bypass capacitance in order to maintain good dc VCC and GND levels.

- All signals from this connector are unbuffered and should not be heavily loaded. A good rule is 2 TTL loads. In addition receivers and drivers should be located near the connector and any connector signal should not run over 4 inches in length from the connector before entering or leaving a driver or receiver.

- Clock generation is especially critical. Keep traces short, ECL routing rules should be followed if possible . Fan out multiple clocks from a single die to minimize loading per clock . Light damping resistors minimize radiation but cause clock distortion, so tune the values carefully.

- Keep in mind current draw on the A3000 is tight so use CMOS and powerdown DRAM modes when possible. New FCT devices use significantly lower current than F and run faster. A local bus card should draw no more than 2Amps @ 5VDC.

- Be aware of heat dissipation issues especially on very high speed microprocessors.

- Noise test local bus cards and ensure good ac signal quality since a nasty signal will get nastier after passing through an inductive connector to the motherboard. And keep in mind that any noise a local card injects into the system will make the entire A3000 less reliable.

- Local bust card mounting holes are plated through to ground on the A3000 motherboard and provide an additional low inductance path to ground. Use this path to minimize ground bounce relative to the motherboard.

# CHAPTER 3

## SIGNAL DESCRIPTIONS

*"There's a name for it*
*And names make all the difference in the world"*
*-David Byrne*

The signals on the Local Bus Slot can be broken down into several categories. Some of these are in common with the 68030, some are specific to this slot. The actual pinout of the connector is detailed in the appendix.

### 3.1 Power Connections

These signals provide digital supply levels to the local bus card. There are quite a few of both levels on the physical connector; generally at least one for every two or three signal pins.

Digital Ground (GND)

This is the digital supply ground used by all digital devices in the system. The local bus card gets GND though its mounting posts as well as the connector pins.

Digital Supply (+5VDC)

This is the digital supply. This is specified as +5VDC ± 5%. The system power budget allocates up to 2Amps for this slot.

### 3.2 System Initialization

These signals are driven by the A3000 motherboard logic to initialize the system; local bus cards

should listen as appropriate.

/RESET

This is an open-collector signal driven by the system reset logic or, indirectly, any CPU device that needs to reset the I/O subsystem. Local bus cards generally don't use this, though it can be used to reset I/O devices or hold the main system in reset if necessary.

/FPURST

This active input is driven by the system reset logic to indicate the full CPU register reset condition.

/CPURST

This open-collector signal is driven by the system reset logic to indicate a full CPU register reset condition to the CPU, and can be driven by the CPU to cause an I/O reset in the rest of the system.

### 3.3 68030 Signals

All of these signals are directly connected to the 68030, and more information on them is available in the 68030 User's Manual. Most of these must be driven or sampled by any local slot DMA device.

Address Bus ($A_{31}..A_0$)

The 32 bit processor address bus, driven by the bus master, tristated by inactive masters.

Data Bus ($D_{31}..D_0$)

The 32 bit processor data bus, driven by the bus master for writes, the slave for reads. This is tristated when outside of a bus cycle (/AS is negated).

Function Codes ($FC_2..FC_0$)

An address bus extension, driven by the bus master, tristated by inactive masters. Most slaves respond only to $FC_0 \oplus FC_1$.

Bus Size ($SIZ_1..SIZ_0$)

Data bus size request, driven by the bus master, tristated by inactive masters.

Cycle Strobes (/AS, /DS)

/AS indicated the start of a bus cycle and valid addresses, /DS indicates valid data for write cycles. Both are driven by the bus master, tristated by inactive bus masters.

Read Indicator (R/W)

Driven by this bus master, this tristated signal is high to indicate a read, low to indicate a write.

Read-Modify-Write Cycle (/RMC)

This line is asserted by the bus master to effect a bus lock; while its active, no bus arbitration takes place, and shared memory coprocessors (except Agnus) stay out of the memory involved in the transaction.

Other Strobes (/ECS, /OCS, /DBEN)

These are additional 68030 stobes that aren't used by the A3000, and therefore, don't have to be driven by a local bus master. They are provided here for the possible use of any slave device that wants them; see the 68030 User's Manual for signal details.

Burst Control (/CBREQ, /CBACK)

The local bus slave drives /CBREQ to indicate that its capable of supporting a burst cycle. The local bus master responds with /CBACK to indicate that it can run a burst cycle.

Cache Control (/CIIN, /CIOUT)

The bus slave drives the /CIIN line to indicate that the currently addressed location is uncachable. The bus master drives /CIOUT to indicate that the current location is uncachable, based on MMU tables as well as /CIIN.

Cycle Termination (/STERM, /$DSACK_1$, /$DSACK_0$, /AVEC).

The bus slave drives either /STERM or one or more /DTACKs to normally terminate a cycles. The combination of DSACK lines indicates the bus port size; /STERM can only be generated by 32-bit-port slaves. The /AVEC line is driven by local bus logic to terminate an interrupt asknowledge cycle with an autovector rather than a device-supplied vector.

Interrupts (/$IPL_2$-$IPL_0$)

Encoded interrupt inputs. These are generally serviced only by the primary bus master, though other schemes are possible with the proper software support. The are inputs; they can't ever be driven by a slave or a master.

Interrupt Pending (/IPEND)

Driven by the 68030 to indicate that there's a pending interrupt to be serviced. A secondary bus master may use this as an indication to let the 68030 back onto the local bus, if the 68030 is handling the interrupts.

Exceptions (/HALT, /BERR)

/HALT driven alone causes the CPU to stop; generally this is used by single-stepping emulators. /HALT driven with /RESET indicates a full 68000 style reset, and is considered archaic on the A3000 local bus. /BERR driven alone indicates some kind of bus error, generally a bus collision or timeout. /BERR and /HALT driven together indicate a bus retry.

### 3.4 Bus Arbitration Signals

These are the signals used to arbitrate the local bus in the ways previously described, supporting both primary and secondary bus masters.

Bus Requests (/BR, /CBR)

The both the /BR and /CBR line cause the bus to be requested from the 68030. The /BR line is for secondary bus masters, and it is a time multiplexed open collector line shared with a similar /BR output from the Buster chip. The /CBR line causes a request to go to the 68030, and once the primary arbitration is completed, the new primary master on the local bus slot must deal with incoming /BRs from Buster.

SCSI Bus Request (/SBR)

This line allows the local bus card to monitor when the SCSI devices wants the bus; this is primarily used as an indicator to secondary masters to give up the local bus.

Bus Grants (/BG, /BG30)

The /BG line is the main local bus grant signal. It is normally generated by the 68030, but when a primary master takes over, this line will tristate, allowing the primary master to drive /BG in response to an incoming /BR. The /BG30 line is the bus grant line coming directly from the 68030 chip.

Bus Grant Acknowledges (/BGACK, /BOSS)

The /BGACK signal is the main bus grant acknowledge, shared by Buster and the DMAC. Secondary masters drive /BGACK to acquire the local bus. The /BOSS signal is a private /BGACK-equivalent to the 68030, used by a primary bus master to acquire the bus from the 68030.

Bus Clear Request (/EBCLR)

This is a signal from the bus arbiter, indicating that some other bus master wants the local bus. This is generally used by a secondary bus master as an indicator of when to get off the bus.

### 3.5 Other Local Bus Signals

Local Slot Memory Decode (/RAMSLOT)

This is an address based chip select for the region of memory allocated to the local bus slot, $08000000-$0fffffff.

Emulator Mode (/EMUL)

This signal can be driven by local bus slot emulator devices to pull the /CDIS and /MMUDIS lines on the 68030, thereby disabling the cache and MMU for debugging purposes.

Cycle Wait (/WAIT)

This line is asserted by a bus monitoring device, such as a cache, to hold off cycle start by either the memory controller (RAMSEY) or expansion bus controller (BUSTER). This gives the device time to determine if it owns that address, retry the cycle, or anything else necessary to support cache and similar kinds of devices.

FPU Chip Select (/FPUCS)

This is a decode for the Coprocessor Device 1, the FPU, generated by the Gary Chip.

### 3.6 Clocks

This section details the A3000 system clocks available at the local bus slot, the clocking alternatives available to a local bus device, and various clock control lines to facilitate this control.

System Clocks ($CPUCLK_A$, CLK90)

These are the main A3000 system clocks. $CPUCLK_A$ is a 16MHz or 25MHz clock, depending on the system configuration, and is the main system, CPU, and FPU clock. CLK90 is CPUCLK shifted 90°.

External Clocks (EXTCLK, EXT90)

These clocks can be driven to replace the on-board clocks to the main system. Some jumpers, described in the appendix, can be arranged to permit the use of these clocks.

### 3.7 New Amiga 3000T Signals

These signals were added to the A3000T Local Bus Slot. They are also available on the A3000+ Local Bus Slot.

System Clock Steal (DIS_CLKS)

This implements an alternate clock replacement method. When the DIS_CLKS line is driven high, the replacement clocks can be driven onto the local bus. This eliminates the need for any jumper adjustments to be made on the motherboard when a clock sourcing board is installed.

Replacement Clocks ($ECPUCLK_A$, $ECPUCLK_B$, ECLK90, $ECLK90_A$)

These are replacement main system clocks, and their 90° counterparts, that can be directly driven onto the local bus when DIS_CLKS is asserted.

CPU Clock Steal (DIS_CLK30, ECLK30)

This allows the 68030 clock to be driven from the local bus, again for skew reduction or other such tricks. When DIS_CLK30 is asserted, ECLK30 can be driven by local bus card logic.

### 3.8 New Amiga 3000+ Signals

Several signals were added to the A3000+ Local Bus Slot. Most of these are all no-connects on the A3000 and A3000T systems.

Slot Type Sense (/SENSEA3P)

This signal allows a card to sense whether it’s installed in an A3000+ or an A3000/A3000T system. The card should connect a 1K resistor to this line. On an A3000 or

A3000T, the line will be high, on an A3000+, it will be low.

Interrupt Out (/INT6)

This is the shared level six interrupt line. It can be driven by a Local Bus Slot device to interrupt the host CPU.

Coprocessor Signals (/CI2P, /PI2C)

These are actually two general purpose lines from the A3000+ Coprocessor Control Register. The /CI2P line is earmarked for a signal from the Coprocessor to the host processor, and the /PI2C line is earmarked for a signal from the host to the Coprocessor. In reality, the lines can be used for any private communications or I/O protocol desired.

# APPENDICES

*"He saw that the hands that build*
*could also pull down...."*

*-U2*

## A.1 Local Bus Connector Pinout

These signals are described in the text. A more complete description of the standard 68030 inputs and outputs is available from the 68030 User's Manual.

The Local Bus Connector is a two piece type, 200 pin, high density connector. It is made by KEL. Be very careful with connection direction and pinout when doing board layouts.

Signals marked with an asterisk (*) are A3000T and A3000+ signals. Signals marked with a plus (+) are A3000+ signals.

| Pin number | Signal name | Pin number | Signal name |
|---|---|---|---|
| 1 | /DSACK$_1$ | 44 | A$_2$ |
| 2 | GND | 45 | A$_{11}$ |
| 3 | GND | 46 | ECLK90 |
| 4 | /HALT | 47 | GND |
| 5 | R/W | 48 | A$_3$ |
| 6 | GND | 49 | A$_{12}$ |
| 7 | GND | 50 | GND |
| 8 | /BGACK | 51 | GND |
| 9 | /SBR | 52 | A$_4$ |
| 10 | GND | 53 | A$_{13}$ |
| 11 | GND | 54 | ECPUCLKB$^*$ |
| 12 | /AVEC | 55 | /WAIT |
| 13 | EXT90 | 56 | A$_5$ |
| 14 | VCC | 57 | A$_{14}$ |
| 15 | VCC | 58 | ECPUCLKA$^*$ |
| 16 | /RAMSLOT | 59 | GND |
| 17 | /BOSS | 60 | A$_6$ |
| 18 | VCC | 61 | A$_{15}$ |
| 19 | VCC | 62 | GND |
| 20 | FC$_0$ | 63 | GND |
| 21 | /STERM | 64 | A$_7$ |
| 22 | VCC | 65 | A$_{16}$ |
| 23 | VCC | 66 | reserved |
| 24 | FC$_1$ | 67 | /CI2P$^+$ |
| 25 | /BR | 68 | A$_{24}$ |
| 26 | VCC | 69 | A$_{17}$ |
| 27 | VCC | 70 | reserved |
| 28 | /CBACK | 71 | GND |
| 29 | /BERR | 72 | A$_{25}$ |
| 30 | DIS_CLKS$^*$ | 73 | A$_{18}$ |
| 31 | /EMUL | 74 | GND |
| 32 | /CBREQ | 75 | GND |
| 33 | A$_8$ | 76 | A$_{26}$ |
| 34 | ECLK30$^*$ | 77 | A$_{19}$ |
| 35 | GND | 78 | DIS_CLK30$^*$ |
| 36 | A$_0$ | 79 | /PI2C$^+$ |
| 37 | A$_9$ | 80 | A$_{27}$ |
| 38 | GND | 81 | A$_{20}$ |
| 39 | GND | 82 | reserved |
| 40 | A$_1$ | 83 | GND |
| 41 | A$_{10}$ | 84 | A$_{28}$ |
| 42 | ECLK90A$^*$ | 85 | A$_{21}$ |
| 43 | /INT6$^+$ | 86 | GND |

| Pin number | Signal name | Pin number | Signal name |
|---|---|---|---|
| 87 | GND | 130 | GND |
| 88 | $A_{29}$ | 131 | GND |
| 89 | $A_{22}$ | 132 | /CIIN |
| 90 | reserved | 133 | /AS |
| 91 | $/DSACK_0$ | 134 | /FPUCS |
| 92 | $A_{30}$ | 135 | $CPUCLK_A$ |
| 93 | $A_{23}$ | 136 | /OCS |
| 94 | VCC | 137 | $D_{31}$ |
| 95 | VCC | 138 | GND |
| 96 | $A_{31}$ | 139 | GND |
| 97 | /DS | 140 | $D_{15}$ |
| 98 | VCC | 141 | $D_{30}$ |
| 99 | VCC | 142 | GND |
| 100 | /ECS | 143 | GND |
| 101 | /CIOUT | 144 | $D_{14}$ |
| 102 | VCC | 145 | $D_{29}$ |
| 103 | VCC | 146 | reserved |
| 104 | /DBEN | 147 | /CBR |
| 105 | /BG | 148 | $D_{13}$ |
| 106 | VCC | 149 | $D_{28}$ |
| 107 | VCC | 150 | reserved |
| 108 | /RMC | 151 | GND |
| 109 | /CPURST | 152 | $D_{12}$ |
| 110 | /FPURST | 153 | $D_{27}$ |
| 111 | reserved | 154 | GND |
| 112 | EXTCPU | 155 | GND |
| 113 | /EBCLR | 156 | $D_{11}$ |
| 114 | $/SENSEZ3P^+$ | 157 | $D_{26}$ |
| 115 | GND | 158 | reserved |
| 116 | /IPEND | 159 | /BG30 |
| 117 | /RESET | 160 | $D_{10}$ |
| 118 | GND | 161 | $D_{25}$ |
| 119 | GND | 162 | reserved |
| 120 | $/IPL_0$ | 163 | GND |
| 121 | $SIZ_0$ | 164 | $D_9$ |
| 122 | GND | 165 | $D_{24}$ |
| 123 | GND | 166 | GND |
| 124 | $/IPL_1$ | 167 | GND |
| 125 | $FC_2$ | 168 | $D_8$ |
| 126 | CLK90 | 169 | $D_{16}$ |
| 127 | reserved | 170 | reserved |
| 128 | $/IPL_2$ | 171 | reserved |
| 129 | $SIZ_1$ | 172 | $D_0$ |

| | |
|---|---|
| 173 | $D_{17}$ |
| 174 | VCC |
| 175 | VCC |
| 176 | $D_{1}$ |
| 177 | $D_{18}$ |
| 178 | VCC |
| 179 | VCC |
| 180 | $D_{2}$ |
| 181 | $D_{19}$ |
| 182 | VCC |
| 183 | VCC |
| 184 | $D_{3}$ |
| 185 | $D_{20}$ |
| 186 | VCC |
| 187 | VCC |
| 188 | $D_{4}$ |
| 189 | $D_{21}$ |
| 190 | GND |
| 191 | GND |
| 192 | $D_{5}$ |
| 193 | $D_{22}$ |
| 194 | GND |
| 195 | GND |
| 196 | $D_{6}$ |
| 197 | $D_{23}$ |
| 198 | GND |
| 199 | GND |
| 200 | $D_{7}$ |

# A.2 CPU/Clock Jumpers

There are various strip-post jumpers (links) on the A3000 family motherboards, which control clock speed, sourcing, and other local slot related features.

### A.2.1 A3000 Jumpers

These are the A3000 clock configuration jumpers. The A3000 can be preconfigured for either 25MHz or 16MHz operation.

**J100** CLK90 Delay Jumper

This jumper has three positions. In position 1-2, it sets up CLK90 for 25MHz operation. In position 2-3, CLK90 is set up for 16MHz operation. In position 3-4, the EXT90 line drives CLK90, rather than the on-board clock logic.

**J102** Board Clock

This jumper has two positions. In position 1-2, the source for CPUCLK$_A$ and CPUCLK$_B$ must be EXTCPU. In position 2-3, it shorts the 68030 and local bus clock sources, such that CPUCLK$_A$, CPUCLK$_B$, and CLK30 all derive from the same source, which is either EXTCPU or the clock based on the local logic, depending on the state of J104.

**J103** FPU Chip Select Jumper

This jumper has three positions. With the shunt on pins 1-2, it disables the on-board FPU. With the shunt in position 2-3, it causes the 68030 to get F-line traps instead of the FPU selection, and in position 3-4 it enables the on-board FPU.

**J104** CPU Clock

This jumper has two positions. In position 1-2, the source for CLK30 is derived from the on-board clock generator. In position 2-3, the source for CLK30 must come from EXTCLK by way of J102.

### A.2.2 A3000T Jumpers

These are the A3000T clock configuration jumpers. The A3000T can be preconfigured for either 25MHz or 16MHz operation.

**J100** CLK90 Delay Jumper
Identical to A3000 J100.

**J102** Board Clock
Identical to A3000 J102.

**J103** FPU Chip Select Jumper
Identical to A3000 J103.

**J104** CPU Clock

Identical to A3000 J104.

**J105** System Clock Disable

In the 2-3 position, this jumper allows the DIS_CLKS line from the Local Bus Slot to operate normally. In the 1-2 position, it forces DIS_CLKS high (asserted), disabling on-board system clock generation.

**J106** CLK90 Short Jumper

In the 2-3 position, there are two versions of CLK90. The system normally runs this way. In the 1-2 position, the two CLK90 lines are shorted together, to allow a single line to source both clocks.

**J107** 68030 Clock Disable

In the 2-3 position, this jumper allows the DIS_CLK30 line from the Local Bus Slot to operate normally. In the 1-2 position, it forces DIS_CLK30 high (asserted), disabling on-board 68030 clock generation.

### A.2.3 A3000+ Jumpers

These are the A3000+ clock configuration jumpers. The A3000+ runs only at 25MHz. Rather than the simple buffer/jumper system of the other A3000 systems, the A3000+ uses a PAL as an intelligent clock generator. This allows it to run clock selectors as logic levels, rather than jumpered clocks, in most cases. This intelligent logic also generates the 50MHz clock for the DSP. This clock will be automatically generated from external clocks rather than the on-board 50MHz clock when an accelerator board is sourcing clocks. Any accelerator setup that removes the clock generator PAL must provide similar functionality on its own.

**J100** CLK90 Delay Jumper

This jumper is similar in function to A3000 J100. In position 1-2, it sets up CLK90 for 25MHz operation. In position 2-3, the EXT90 line drives CLK90, rather than the onboard clock logic. Unlike A3000 J100, this jumper is a logic-level switch to the A3000+ clock generator, no clock lines are routed though it.

**J102** Board Clock

This jumper is identical in function to A3000 J102, though its a logic-level switch to the A3000+ clock generator; no clock lines are routed through it.

**J103** FPU Chip Select Jumper

This jumper is similar in function to A3000 J103. With the shunt on pins 1-2, it enables the on-board FPU. With the shunt in position 2-3, it disables the on-board FPU.

**J104** CPU Clock

This jumper is identical in function to A3000 J104, though it’s a logic-level switch to the A3000+ clock generator; no clock lines are routed through it.

**J105** System Clock Disable
Identical to A3000T J105.

**J107** 68030 Clock Disable
Identical to A3000T J107.

## A.3 References

Motorola, *MC68030 Enhanced 32-Bit Microprocessor User's Manual*, second edition, Motorola Inc. number MC68030UM/AD REV1.

Commodore-Amiga, *The Zorro III Expansion Bus Specification.*

Commodore-Amiga, *The A500/A2000 Technical Reference Manual.*